Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1 (Currently amended). A microprocessor, comprising:

~~a branch unit to process branch instructions and provide a fetch unit with a next instruction address;~~

~~a load/store unit (LSU) to retrieve data from and stored data to a data memory of the microprocessor;~~

~~an arithmetic logic unit (ALU) to performing arithmetic operations on scalar, integer data; and~~

a vector unit to execute a vector instruction to perform a first operation on a first set of ~~data~~ operands and a second operation on a second set of operands[[,]] ~~wherein the first and second operations differ;~~

a vector register file comprising a primary register file and a secondary register file;

wherein the vector instruction includes a first register field indicative of a first primary register in the primary register file and a first secondary register in the secondary register file, a second register field indicative of a second primary register in the primary register file and a second secondary register in the secondary register file, and a third register field indicative of a third primary register in the primary register file and a third secondary register in the secondary register file; and

wherein the first set of operands includes a first operand selected from the first primary register or the first secondary register, a second operand selected from the second primary register or the second secondary register, and a third operand selected from the third primary register or the third secondary register.

2-3 (Canceled).

4 (Currently amended). The microprocessor of claim ~~3~~ 1, wherein the vector unit includes a 3-input primary ~~floating point~~ unit and a 3-input secondary ~~floating point~~ unit, wherein the [[3-input]] primary ~~floating point~~ unit is configured to perform ~~a floating point~~ the first operation on the first set of operands and the 3-input secondary ~~floating point~~ unit is configured to perform a ~~floating point~~ the second operation on the second set of operands.

5-6 (Canceled).

7 (Currently amended). The microprocessor of claim [[2]] 1, wherein ~~the vector unit is further characterized as being enabled to perform a cross instruction in which~~ the first and second operations ~~both~~ use at least one operand from the primary register file and at least one operand from the secondary register file.

8 (Currently amended). The microprocessor of claim [[2]] 1, wherein ~~the vector unit is further characterized as being enabled to perform a cross replicate vector instruction in which~~ the first and second ~~operations are both performed using~~ sets of operands include at least one common operand.

9 (Currently amended). The microprocessor of claim [[2]] 1, wherein the vector ~~unit is configured to store~~ register file contains information representing a real portion of a complex number in the primary register file and an imaginary portion of the complex number in the secondary register file.

10 (Currently amended). The microprocessor of claim 9, wherein the vector unit is configured to execute a complex computation instruction in which the imaginary portion of the first operand of the first set of operands is multiplied by an imaginary portion of a second operand in the first operation and in which the imaginary portion of the first operand is multiplied by a real portion of the second operand in the second operation.

11-20 (Canceled).

21 (New). The microprocessor of claim 1, wherein the second set of operands include a first operand selected from the first primary register or the first secondary register, a second operand selected from the second primary register or the second secondary register, and a third operand selected from the third primary register or the third secondary register.

22 (New). The microprocessor of claim 4, wherein the first operation includes multiplying two of the three first set of operands to obtain a first product and adding or subtracting the remaining of the first set of operand to or from the first product and wherein the second operation includes multiplying two of the three second set of operands to obtain a second product and adding or subtracting the remaining of the second set of operands to or from the second product.

23 (New). The microprocessor of claim 22, wherein the first and second sets of operands comprise first and second sets of floating point formatted operands.

24 (New). The microprocessor of claim 1, wherein the vector register file wherein the vector instruction includes a target register field indicative of a primary target register in the primary register file and a secondary target register in the secondary register file and further wherein the

vector unit is further configured to store a result of the first operation in the primary target register and to store a result of the second operation in the secondary target register.

25 (New). A vector unit to process a vector instruction having an opcode and first, second, and third register fields, comprising:

a register file including a primary register file having a set of primary registers and a secondary register file having a set of secondary registers, wherein each register field identifies a register in the primary register file and a corresponding register in the secondary register file;

primary and secondary calculating units, wherein the primary calculating unit includes first, second, and third inputs to receive, respectively, first, second, and third operands of a first set of operands and wherein the secondary calculating unit includes first, second, and third inputs to receive, respectively, first, second, and third operands of a second set of operands; and

multiplexing circuitry controlled by the opcode to select each of the first, second, and third operands in the first and second set of operands from the set of primary and secondary file registers identified by the register fields.

26. (New). The vector unit of claim 25, wherein the multiplexing circuitry is controlled by the opcode to select:

the first operand in the first set of operands from either the first primary or the first secondary registers;
the second operand in the first set of operands from either the second primary or the second secondary registers; and
the third operand in the first set of operands from either the third primary or the third secondary registers;
the first operand in the second set of operands from either the first primary or the first secondary registers,
the second operand in the second set of operands from either the second primary or the second secondary registers; and
the third operand in the second set of operands from either the third primary or the third secondary registers

27. (New) The vector unit of claim 25, wherein the primary calculating unit is controlled by the opcode to perform a first operation on the first set of operands and the secondary calculating unit is controlled by the opcode to perform a second operation on the second set of operands.

28. (New) The vector unit of claim 27, wherein the first operation differs from the second operation.

29. (New) The vector unit of claim 27, wherein the first and second operations both include multiplying their respective first and third operands to obtain respective first products and adding or subtracting their respective second operands to or from the respective first products.

30. (New) The vector unit of claim 25, wherein the first, second, and third operands of the first and second sets of operands are all floating point formatted operands.

31 (New). A microprocessor including:

an execution unit enabled to execute an asymmetric instruction, wherein the asymmetric instruction includes a set of three operand register fields and a target register field and an operation code (opcode);

a register file accessible by the execution unit and having a rank of two including a primary register file and a secondary register file wherein a value in an operand register field identifies a register in the primary register file and a corresponding register in the secondary register file;

wherein the execution unit is configured to perform a first operation on a first set of three operands selected from registers identified by the set of operand register fields and to perform a second operation on a second set of three operands also selected from the registers identified by the set of operand registers fields wherein the first and second operations and selection of the first and second sets of operands are determined by the opcode.

32 (New). The microprocessor of claim 31, wherein at least one condition selected from the group of conditions consisting of the first and second operations being different and the first and second sets of operands being different is true.

33 (New). The microprocessor of claim 31, wherein the execution unit is further configured to store a result of the first operation in a register of the primary register file determined by the target register field and the result of the second operation in a register of the secondary register field also determined by the target register field.

34 (New). The microprocessor of claim 31, including multiplexing circuitry controlled by the opcode to select a first of the first set of three operands from a first primary and a first secondary register identified by a first operand register field, a second of the first set of three operands from a second primary and a second secondary register identified by a second operand register field, a third of the first set of three operands from a third primary and a third secondary register identified by a first operand register field, a first of the second set of three operands from a first primary and a first secondary register identified by a first operand register field, a second of the

second set of three operands from a second primary and a second secondary register identified by a second operand register field, and a third of the second set of three operands from a third primary and a third secondary register identified by a first operand register field.